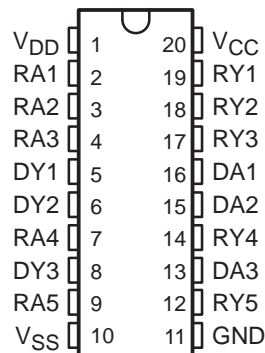


- **Single Chip With Easy Interface Between UART and Serial-Port Connector of IBM™ PC/AT™ and Compatibles**
- **Meets or Exceeds the Requirements of ANSI Standard TIA/EIA-232-F and ITU Recommendation V.28**
- **Designed to Support Data Rates up to 120 kbit/s**
- **Pinout Compatible With SN75C185 and SN75185**
- **ESD Protection to 2 kV on Bus Terminals**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB) Packages, and DIPs (N)**

**DB, DW, OR N PACKAGE
(TOP VIEW)**



description

The GD75232 combines three drivers and five receivers from TI™ trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of an IBM™ PC/AT™ and compatibles. The bipolar circuits and processing of the GD75232 provide a rugged, low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

The GD75232 complies with the requirements of the TIA/EIA-232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and a peripheral at signaling rates up to 20 kbit/s. The switching speeds of the GD75232 are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be expected unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates up to 120 kbit/s, use of ANSI TIA/EIA-423-B (ITU V.10) and TIA/EIA-422-B (ITU V.11) standards is recommended.

The GD75232 is characterized for operation over the temperature range of 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TI is a trademark of Texas Instruments Incorporated.
IBM and PC/AT are trademarks of International Business Machines Corporation.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



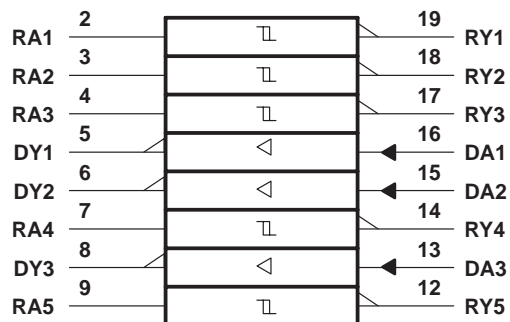
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated

GD75232 MULTIPLE RS-232 DRIVERS AND RECEIVERS

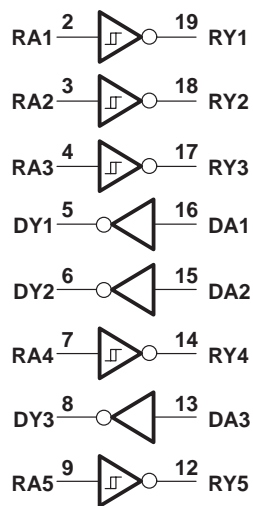
SLLS206C – MAY 1995 – REVISED JULY 1998

logic symbol†

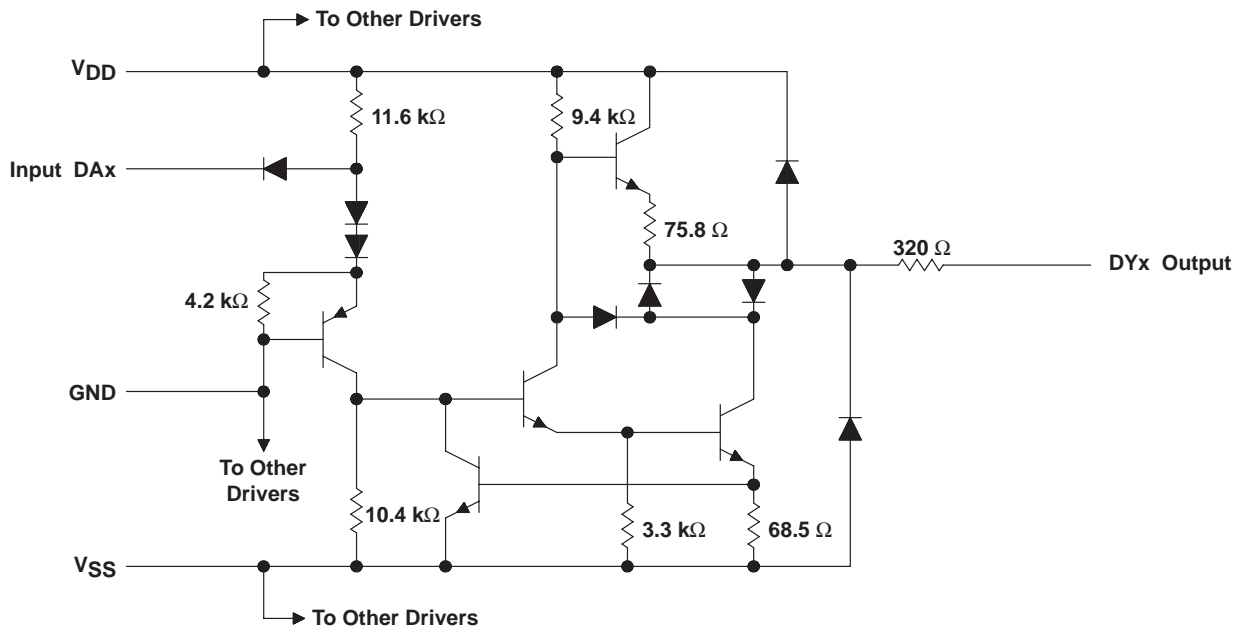


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

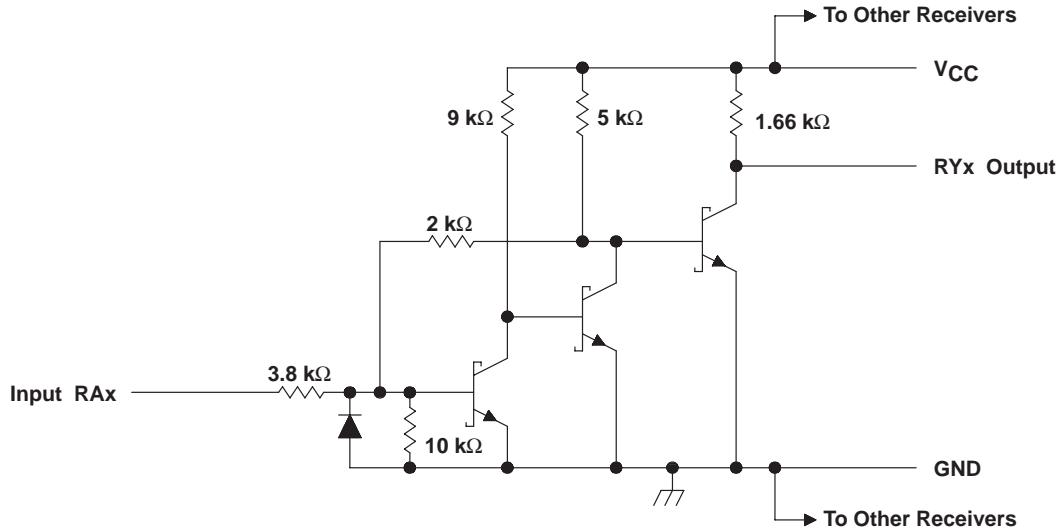


schematic (each driver)



Resistor values shown are nominal.

schematic (each receiver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	10 V
Supply voltage, V_{DD} (see Note 1)	15 V
Supply voltage, V_{SS} (see Note 1)	-15 V
Input voltage range, V_i : Driver	-15 V to 7 V
Receiver	-30 V to 30 V
Driver output voltage range, V_O	-15 V to 15 V
Receiver low-level output current, I_{OL}	20 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	115°C/W
DW package	97°C/W
N package	67°C/W
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to the network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

GD75232

MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS206C – MAY 1995 – REVISED JULY 1998

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		7.5	9	15	V
Supply voltage, V_{SS}		-7.5	-9	-15	V
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH} (driver only)		1.9			V
Low-level input voltage, V_{IL} (driver only)				0.8	V
High-level output current, I_{OH}	Driver			-6	mA
	Receiver			-0.5	
Low-level output current, I_{OL}	Driver			6	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

supply currents over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
I_{DD} Supply current from V_{DD}	All inputs at 1.9 V, No load	$V_{DD} = 9\text{ V}, V_{SS} = -9\text{ V}$		15	mA
		$V_{DD} = 12\text{ V}, V_{SS} = -12\text{ V}$		19	
		$V_{DD} = 15\text{ V}, V_{SS} = -15\text{ V}$		25	
	All inputs at 0.8 V, No load	$V_{DD} = 9\text{ V}, V_{SS} = -9\text{ V}$		4.5	mA
		$V_{DD} = 12\text{ V}, V_{SS} = -12\text{ V}$		5.5	
		$V_{DD} = 15\text{ V}, V_{SS} = -15\text{ V}$		9	
I_{SS} Supply current from V_{SS}	All inputs at 1.9 V, No load	$V_{DD} = 9\text{ V}, V_{SS} = -9\text{ V}$		-15	mA
		$V_{DD} = 12\text{ V}, V_{SS} = -12\text{ V}$		-19	
		$V_{DD} = 15\text{ V}, V_{SS} = -15\text{ V}$		-25	
	All inputs at 0.8 V, No load	$V_{DD} = 9\text{ V}, V_{SS} = -9\text{ V}$		-3.2	mA
		$V_{DD} = 12\text{ V}, V_{SS} = -12\text{ V}$		-3.2	
		$V_{DD} = 15\text{ V}, V_{SS} = -15\text{ V}$		-3.2	
I_{CC} Supply current from V_{CC}	$V_{CC} = 5\text{ V},$	All inputs at 5,	No load	30	mA



DRIVER SECTION

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 9\text{ V}$, $V_{SS} = -9\text{ V}$, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_{IL} = 0.8\text{ V}$, $R_L = 3\text{ k}\Omega$, See Figure 1	6	7.5		V
V_{OL}	Low-level output voltage (see Note 3)	$V_{IH} = 1.9\text{ V}$, $R_L = 3\text{ k}\Omega$, See Figure 1		-7.5	-6	V
I_{IH}	High-level input current	$V_I = 5\text{ V}$, See Figure 2			10	μA
I_{IL}	Low-level input current	$V_I = 0$, See Figure 2			-1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (see Note 4)	$V_{IL} = 0.8\text{ V}$, $V_O = 0$, See Figure 1	-4.5	-12	-19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	$V_{IH} = 2\text{ V}$, $V_O = 0$, See Figure 1	4.5	12	19.5	mA
r_O	Output resistance (see Note 5)	$V_{CC} = V_{DD} = V_{SS} = 0$, $V_O = -2\text{ V to } 2\text{ V}$	300			Ω

- NOTES: 3. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if -10 V is maximum, the typical value is a more negative voltage).
 4. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
 5. Test conditions are those specified by TIA/EIA-232-F and as listed above.

switching characteristics, $V_{CC} = 5\text{ V}$, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$R_L = 3\text{ k}\Omega\text{ to } 7\text{ k}\Omega$, $C_L = 15\text{ pF}$, See Figure 3		315	500	ns
t_{PHL}	Propagation delay time, high- to low-level output			75	175	ns
t_{TLH}	Transition time, low- to high-level output	$R_L = 3\text{ k}\Omega\text{ to } 7\text{ k}\Omega$, $C_L = 15\text{ pF}$, See Figure 3		60	100	ns
		$R_L = 3\text{ k}\Omega\text{ to } 7\text{ k}\Omega$, $C_L = 2500\text{ pF}$, See Figure 3 and Note 6		1.7	2.5	μs
t_{THL}	Transition time, high- to low-level output	$R_L = 3\text{ k}\Omega\text{ to } 7\text{ k}\Omega$, $C_L = 15\text{ pF}$, See Figure 3		40	75	ns
		$R_L = 3\text{ k}\Omega\text{ to } 7\text{ k}\Omega$, $C_L = 2500\text{ pF}$, See Figure 3 and Note 6		1.5	2.5	μs

NOTE 6: Measured between $\pm 3\text{-V}$ and $\pm 3\text{-V}$ points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied either high or low.

GD75232

MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS206C – MAY 1995 – REVISED JULY 1998

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V _{IT+}	Positive-going input threshold voltage	See Figure 5	T _A = 25°C	1.75	1.9	2.3	V
			T _A = 0°C to 70 °C	1.55		2.3	
V _{IT-}	Negative-going input threshold voltage		0.75	0.97	1.25		
V _{hys}	Input hysteresis voltage (V _{IT+} - V _{IT-})		0.5				
V _{OH}	High-level output voltage	I _{OH} = -0.5 mA	V _{IH} = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V _{OL}	Low-level input voltage	I _{OL} = 10 mA, V _I = 3 V		0.2	0.45	V	
I _{IH}	High-level input current	V _I = 25 V, See Figure 5	3.6		8.3	mA	
		V _I = 3 V, See Figure 5	0.43				
I _{IL}	Low-level output current	V _I = -25 V, See Figure 5	-3.6		-8.3	mA	
		V _I = -3 V, See Figure 5	-0.43				
I _{OS}	Short-circuit output current	See Figure 4		-3.4	-12	mA	

† All typical values are at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 9 V, and V_{SS} = -9 V.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = -12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 50 pF, R _L = 5 kΩ, See Figure 6		107	250	ns
t _{PHL}	Propagation delay time, high- to low-level output			42	150	ns
t _{TLH}	Transition time, low- to high-level output			175	350	ns
t _{THL}	Transition time, high- to low-level output			16	60	ns
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 15 pF, R _L = 1.5 kΩ, See Figure 6		100	160	ns
t _{PHL}	Propagation delay time, high- to low-level output			60	100	ns
t _{TLH}	Transition time, low- to high-level output			90	175	ns
t _{THL}	Transition time, high- to low-level output			15	50	ns



PARAMETER MEASUREMENT INFORMATION

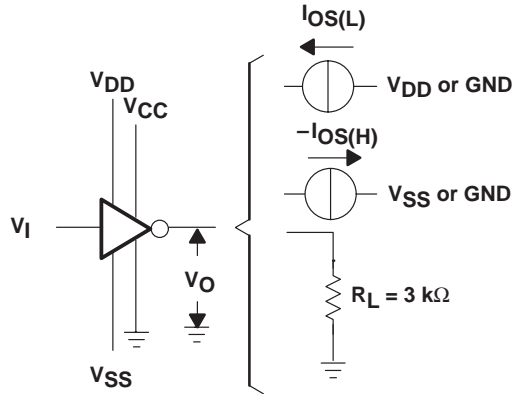


Figure 1. Driver Test Circuit for V_{OH} , V_{OL} , $I_{OS(H)}$, and $I_{OS(L)}$

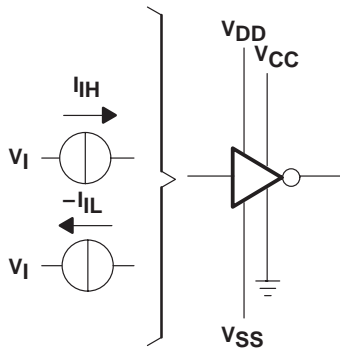
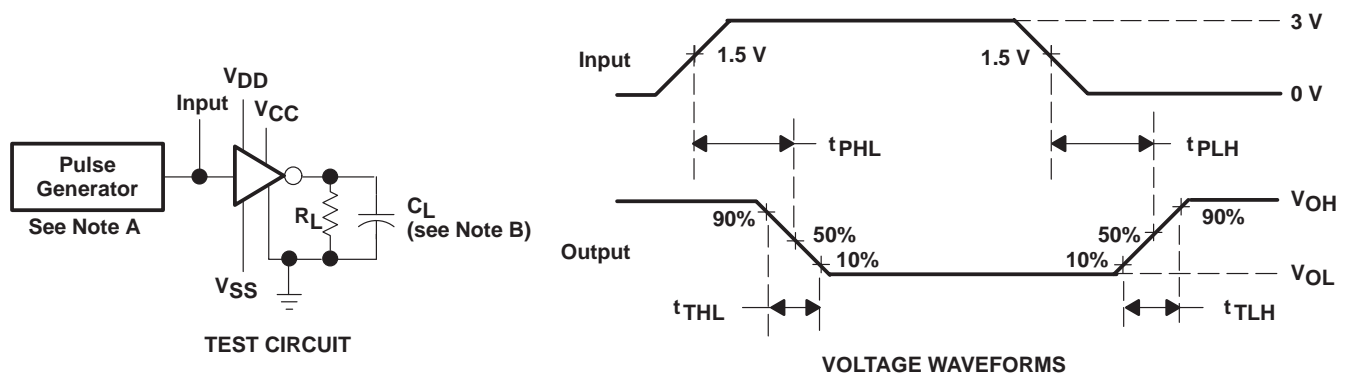


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



NOTES: A. The pulse generator has the following characteristics: $t_w = 25\ \mu\text{s}$, $\text{PRR} = 20\ \text{kHz}$, $Z_O = 50\ \Omega$, $t_r = t_f < 50\ \text{ns}$.
 B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

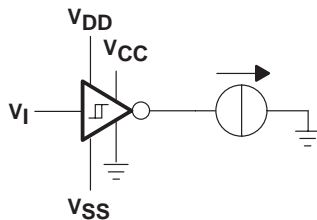


Figure 4. Receiver Test Circuit for I_{OS}

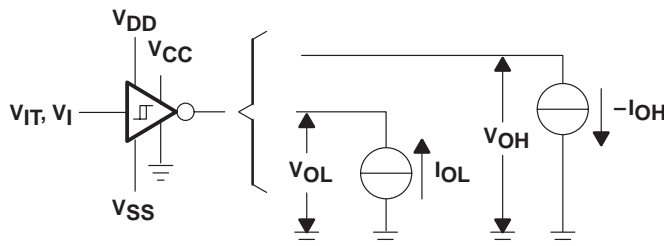
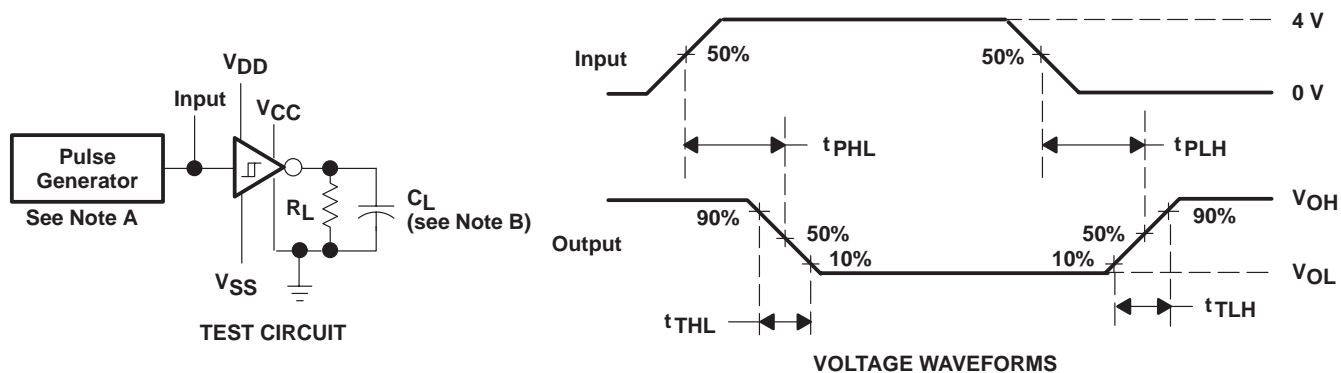


Figure 5. Receiver Test Circuit for V_{IT} , V_{OH} , and V_{OL}



NOTES: A. The pulse generator has the following characteristics: $t_w = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f < 50 \text{ ns}$.
 B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

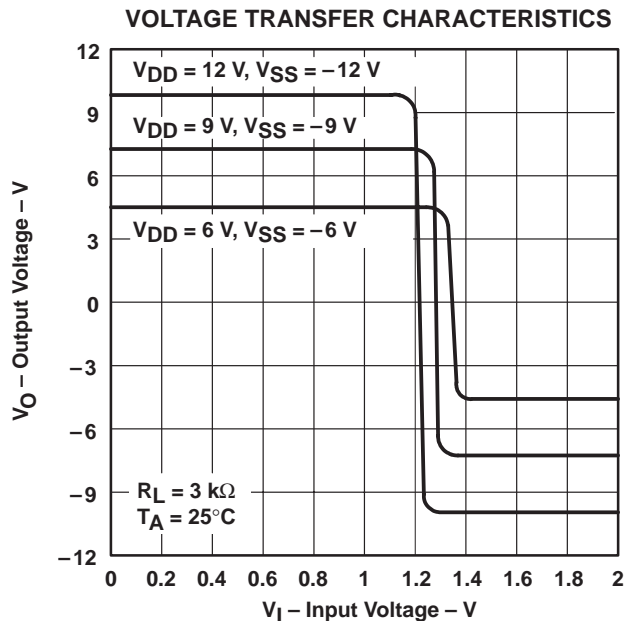


Figure 7

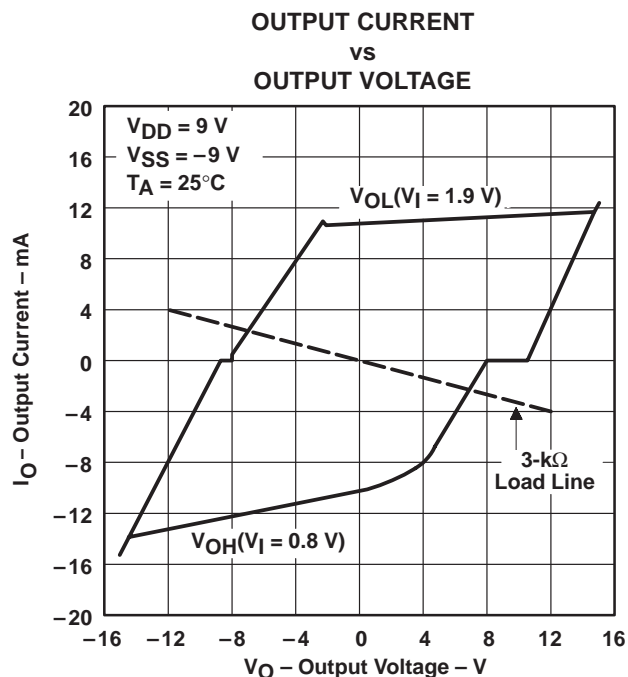


Figure 8

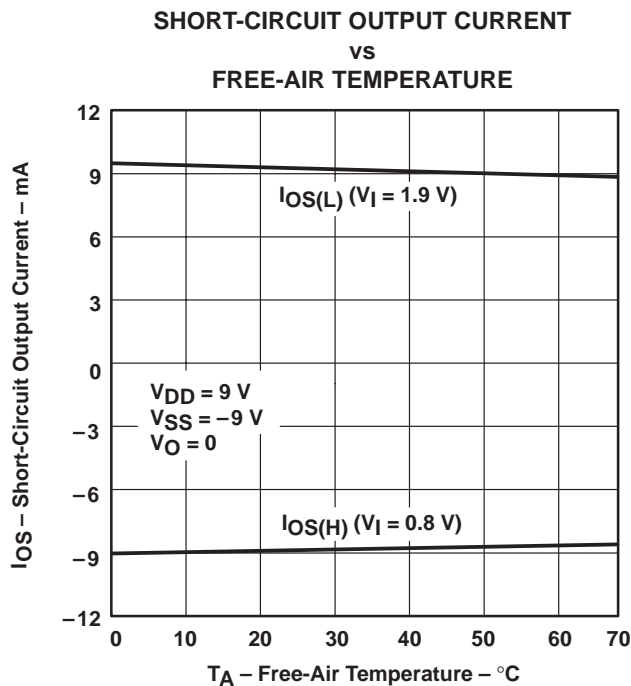


Figure 9

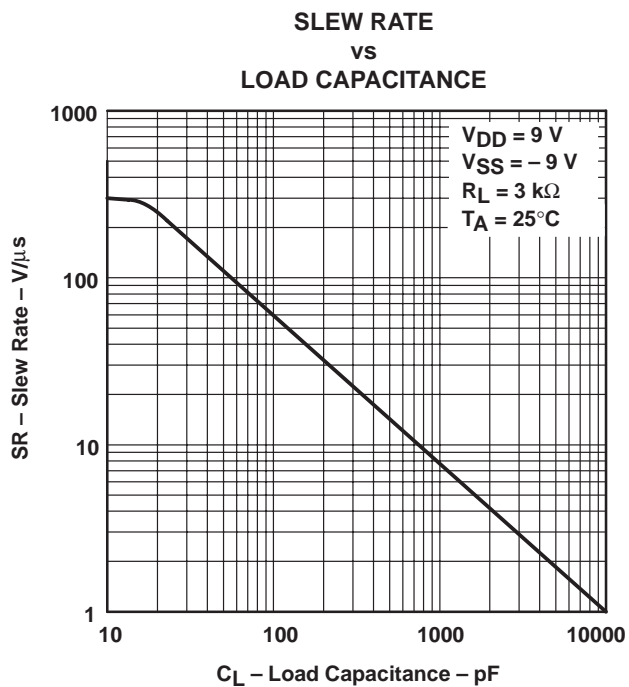


Figure 10

TYPICAL CHARACTERISTICS

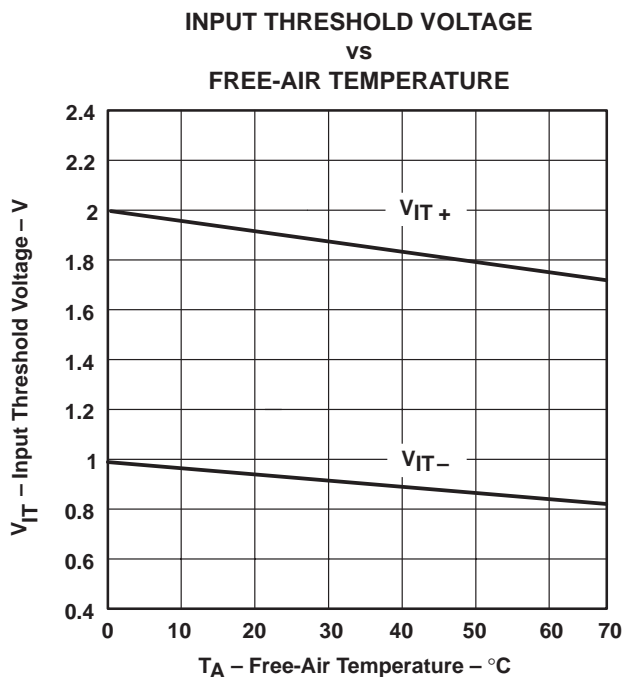


Figure 11

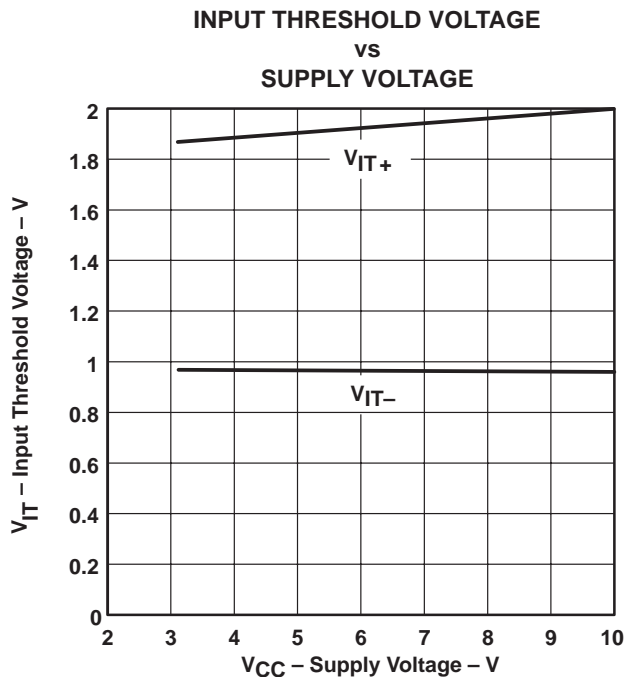
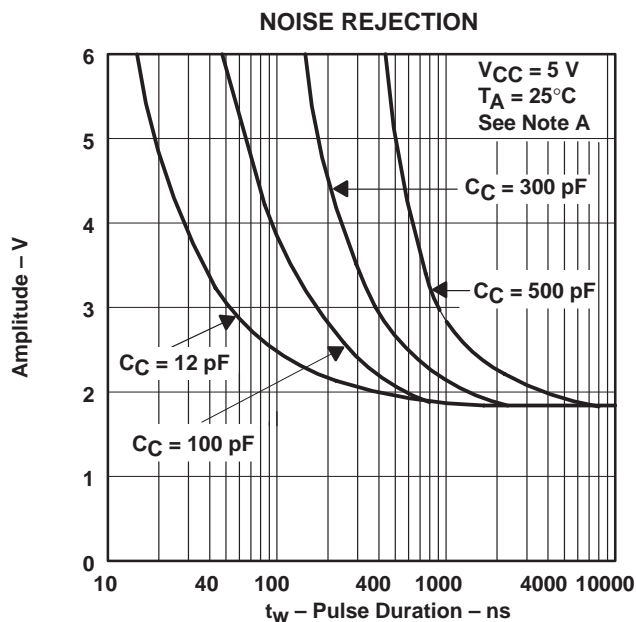


Figure 12



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, does not cause a change of the output level.

Figure 13

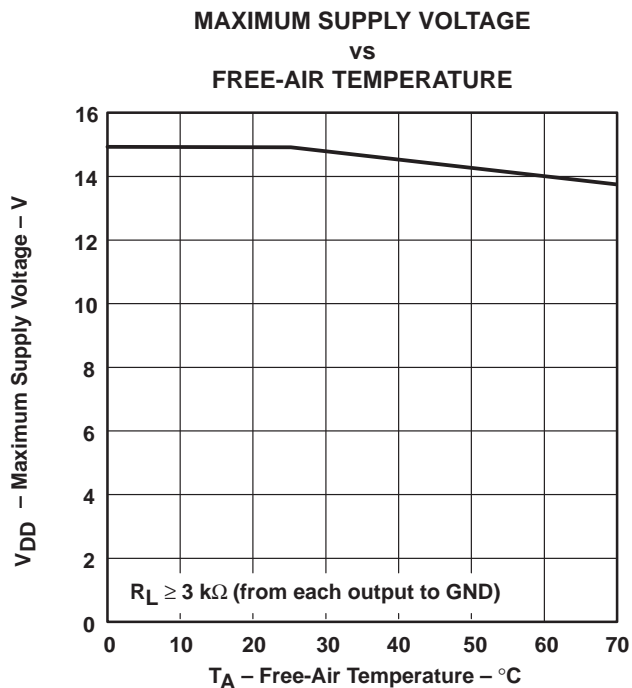


Figure 14

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the GD75232 in the fault condition in which the device outputs are shorted to ± 15 V and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

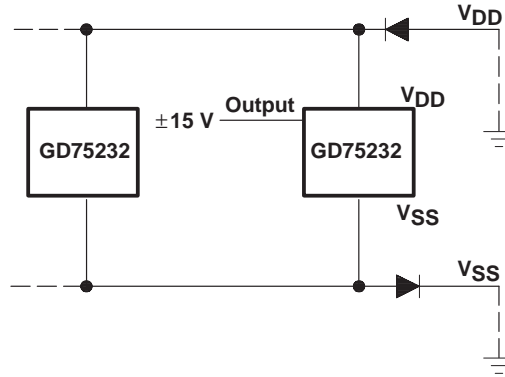


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F

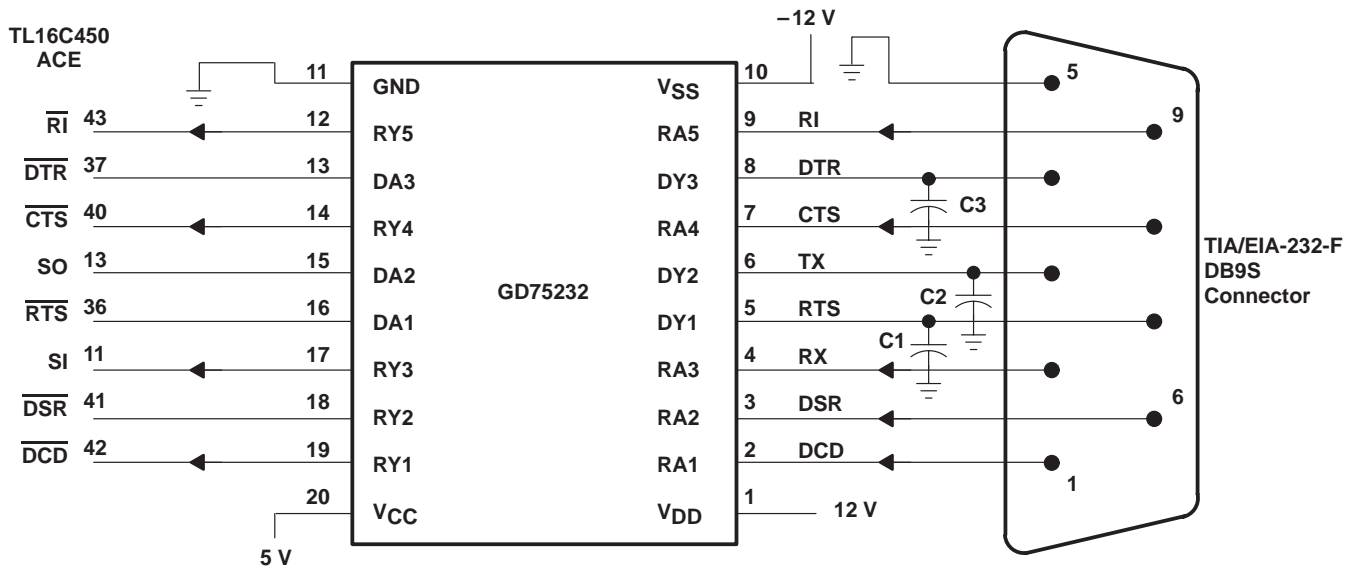


Figure 16. Typical Connection

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.