

Display Elektronik GmbH

DATA SHEET

STANDARD OLED/PLED

DEP 160128A - RGB



Product Specification

Version : 01

08.10.2008

History of Version

Version	Contents	Date	Note
01	NEW VERSION	2008/10/08	SPEC.

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1. Numbering System

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	160x128xRGB	dots
Module dimension (L*W*H)	42.7*33.4*2.025(MAX)	mm
Active area	35.015*28.012	mm
Dot size	0.048(W)x0.199(H)	mm
Dot pitch	0.073(W)x0.219 (H)	mm
Color	262K	

(2) Controller IC: SSD1353 Controller

(3) Temperature Range

Operating	-40 ~ +70
Storage	-40 ~ +85

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	-	+70	
Storage Temperature	TST	-40	-	+85	
Humidity		-	-	85	%
Supply Voltage For Logic	VDD	-0.3	-	3.5	V
Supply Voltage For Panel	Vcc	10	-	21	V
Operating lifetime(blue)			13700(*)		Hrs

*:80cd/m² light on

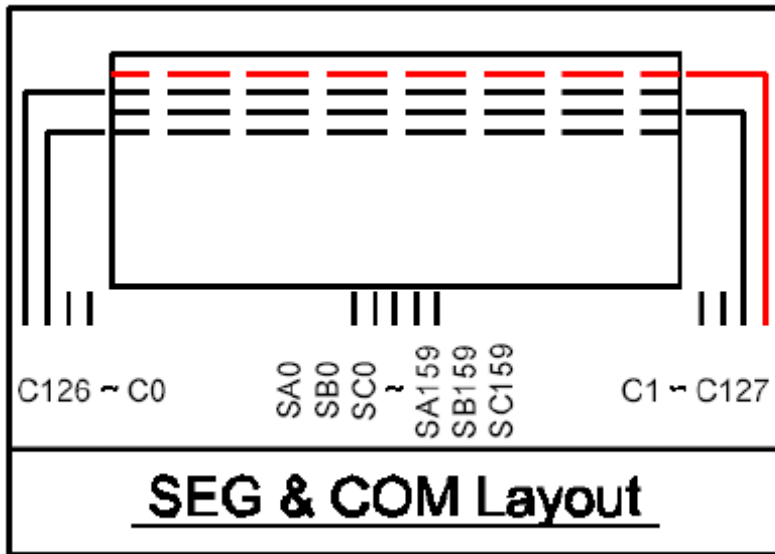
4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	$V_{DD}-V_{SS}$	-	2.4	3.3	3.5	V
Supply Voltage For Panel	$V_{CC}-V_{SS}$	-	16.5	17	17.5	V
Input High Vol	V_{IH}	-	$0.8V_{DD}$	-	V_{DD}	V
Input Low Vol	V_{IL}	-	0	-	$0.2V_{DD}$	V
Output High Vol	V_{OH}	-	$0.9V_{DD}$	-	V_{DD}	V
Output Low Vol.	V_{OL}	-	0	-	$0.1V_{DD}$	V
Supply Current For Logic (with built-in positive voltage)	I_{DD}	-	-	165	-	mA
Supply Current For Logic (without positive voltage)	I_{DD}	-	-	38	-	mA

5. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	160	-	-	deg
Dark Room contrast	2000:1	-	-	-
Response Time	-	10	-	us

6. Panel Layout Diagram



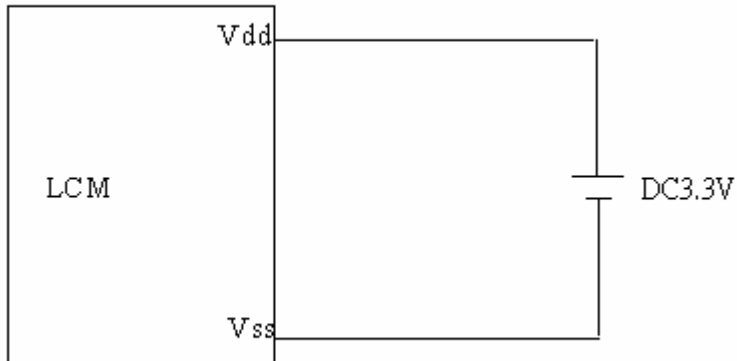
7. Interface Pin Function

Pin No.	Symbol	Level	Description
1	V _{ss}	0V	Ground
2	V _{dd}	3.3V	Supply voltage for logic
3	CS	H/L	Chip select pin
4	/RES	H/L	Hardware Reset pin
5	D/C	H/L	H: Data; L: Command.
6	RW	H/L	8080: data write enable pin 6800: Read/Write select pin
7	E	H/L	8080: data read enable pin 6800: Read/Write enable pin
8	DB0	H/L	Data bus line
9	DB1	H/L	Data bus line
10	DB2	H/L	Data bus line
11	DB3	H/L	Data bus line
12	DB4	H/L	Data bus line
13	DB5	H/L	Data bus line
14	DB6	H/L	Data bus line
15	DB7	H/L	Data bus line
16	DISPOFF/ VCC	- H/L	DISPOFF: Active L VCC: Analog power control (DC 17V)

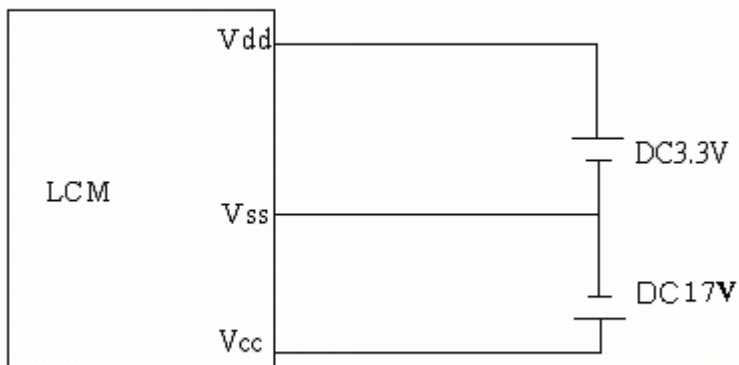
Default:8080 series interface

8. Power Supply For LCD Module

* LCM operating on "DC 3.3V " input with built-in positive voltage



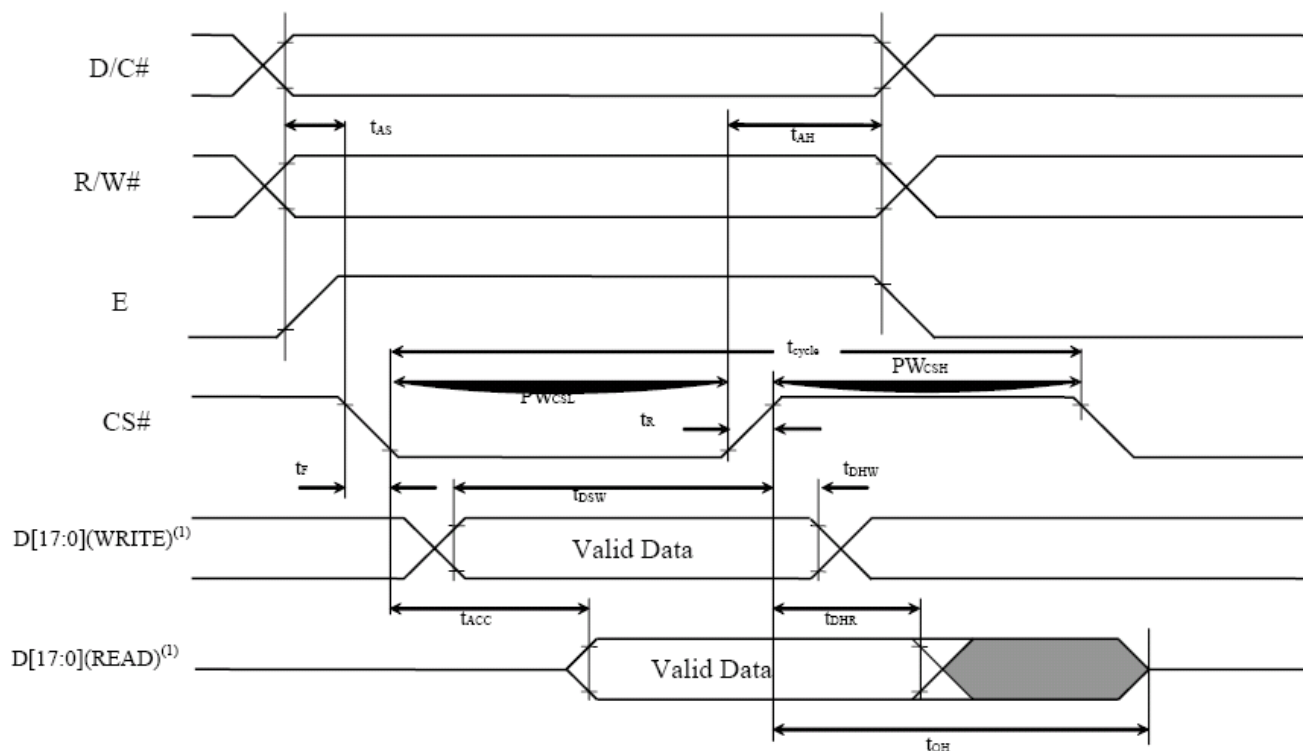
* (Optional) LCM operating on " DC 3.3V " input with external positive voltage.



9. Timing Characteristics

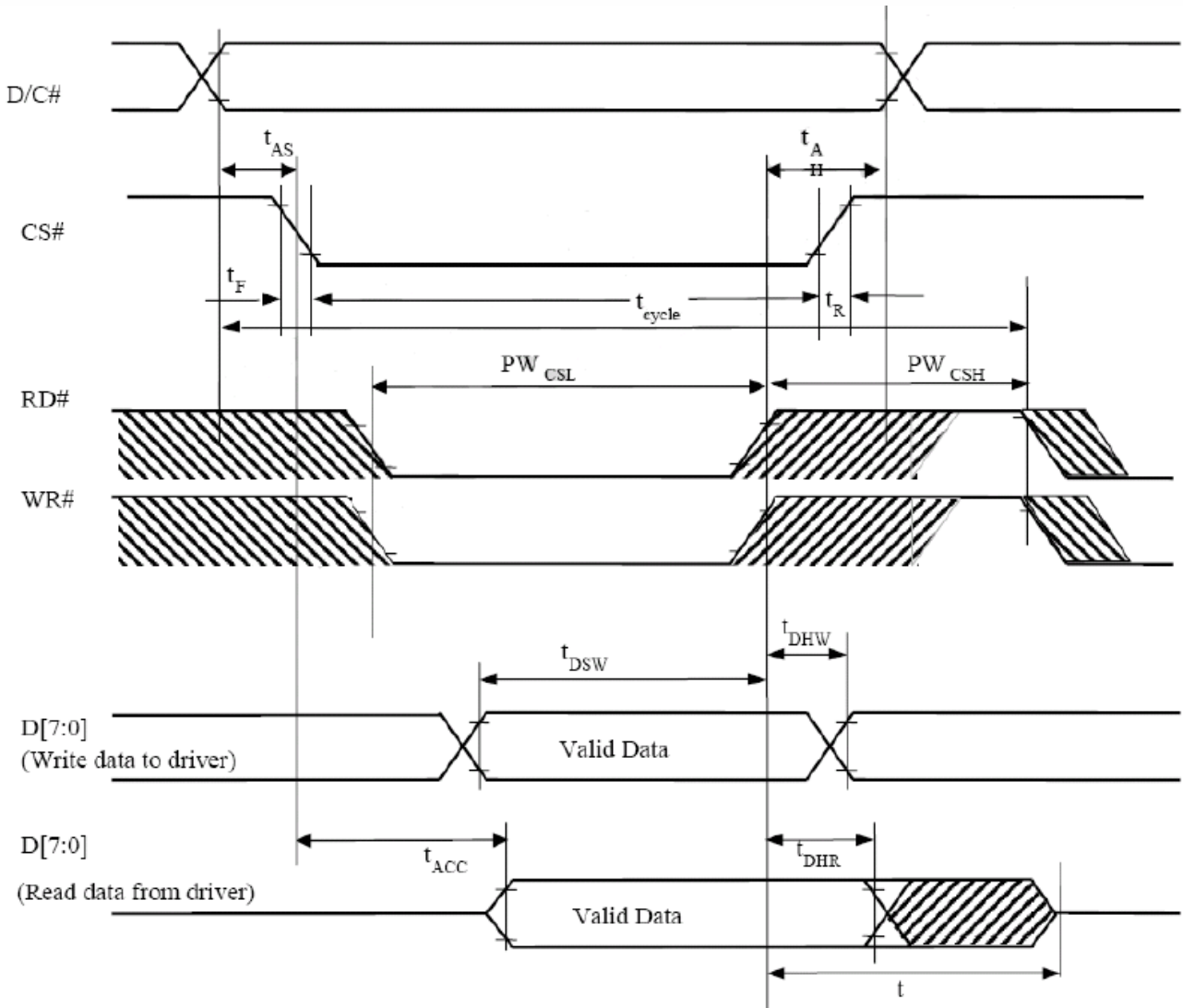
9-1.6800 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_{R}	Rise Time	-	-	15	ns
t_{F}	Fall Time	-	-	15	ns



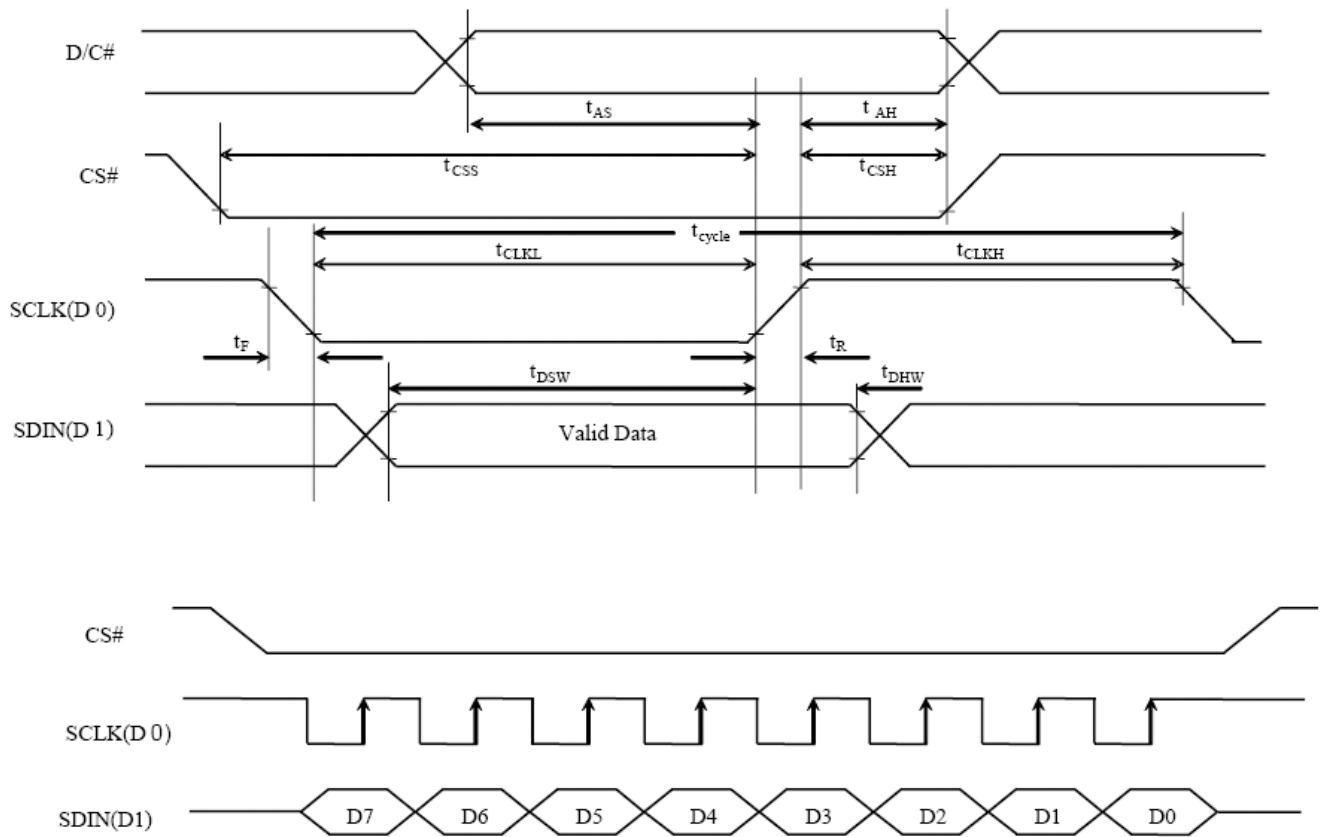
9-2.8080 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLr}	Read Low Time	150	-	-	ns
t_{PWLw}	Write Low Time	60	-	-	ns
t_{PWHr}	Read High Time	60	-	-	ns
t_{PWHw}	Write High Time	60	-	-	ns
t_r	Rise Time	-	-	15	ns
t_f	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns



9-3.Serial Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

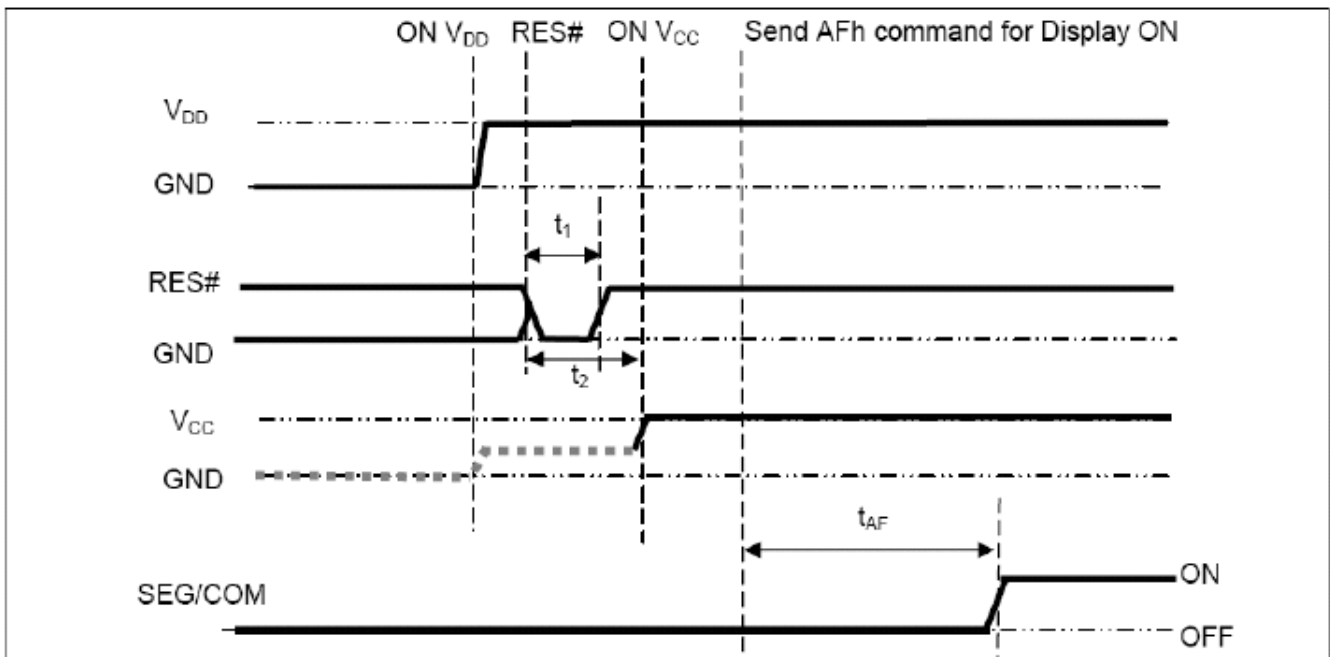


10. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

10.1 POWER ON / OFF SEQUENCE

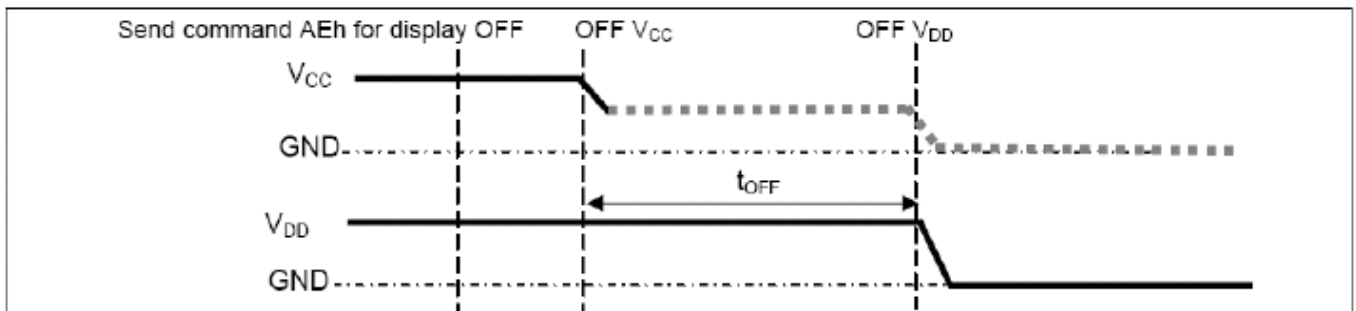
Power ON sequence:

1. Power ON V_{DD} .
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 100us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t_2).Then Power ON V_{CC} .(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V_{CC} . (1), (2)
4. Wait for t_{OFF} . Power OFF V_{DD} . (where Minimum t_{OFF} =0ms, Typical t_{OFF} =100ms)



Note:

- (1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} , V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
- (2) V_{CC} should be disabled when it is OFF.

11. Display Control Instruction

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1	15 A[7:0] B[7:0]	0 A ₇ B ₇	0 A ₆ B ₆	0 A ₅ B ₅	1 A ₄ B ₄	0 A ₃ B ₃	1 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Column Address	Set Column start and end address A[7:0]: Set start column address from 00d-159d [reset= 0d (00h)] B[7:0]: Set end column address from 00d-159d [reset= 159d (9Fh)]
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	75 A[7:0] B[7:0]	0 A ₇ B ₇	1 A ₆ B ₆	1 A ₅ B ₅	1 A ₄ B ₄	0 A ₃ B ₃	1 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Row Address	Set Row start and end address A[7:0]: Set start row address from 00d-131d [reset= 0d (00h)] B[7:0]: Set end row address from 00d-131d [reset= 131d (83h)]
0 1	81 A[7:0]	1 A ₇	0 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Contrast for Color "A"	Set contrast for all color "A" segment (Pins :SA0 – SA159) A[7:0] valid range: 00d to 255d [reset=128d (80h)]
0 1	82 A[7:0]	1 A ₇	0 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀	Set Contrast for Color "B"	Set contrast for all color "B" segment (Pins :SB0 – SB159) A[7:0] valid range: 00d to 255d [reset=128d (80h)]
0 1	83 A[7:0]	1 A ₇	0 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Set Contrast for Color "C"	Set contrast for all color "C" segment (Pins :SC0 – SC159) A[7:0] valid range: 00d to 255d [reset=128d (80h)]
0 1	87 A[3:0]	1 *	0 *	0 *	0 *	0 A ₃	1 A ₂	1 A ₁	1 A ₀	Master Current Control	Set master current attenuation factor A[3:0] can be set from 00d to 15d corresponding to 1/16, 2/16... to 16/16 attenuation. [reset= 15d (0Fh)]

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	8A A[1:0]	1 0	0 0	0 0	0 0	1 0	0 0	1 A ₁	0 A ₀	Set Second Pre-charge speed	Set Second Pre-charge speed A[1:0]= 00b, Second Pre-charge speed =slowest A[1:0]= 01b, Second Pre-charge speed =slow A[1:0]= 10b, Second Pre-charge speed =normal [reset] A[1:0]= 11b, Second Pre-charge speed =Fast
0 1	A0 A[7:0]	1 A ₇	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	0 A ₀	Remap & Color Depth setting	Set driver remap and color depth A[0]=0, Horizontal address increment [reset] A[0]=1, Vertical address increment A[1]=0, RAM Column 0 to 159 maps to Pin SEG (SA,SB,SC) 0 to 159 [reset] A[1]=1, RAM Column 0 to 159 maps to Pin SEG (SA,SB,SC) 159 to 0 A[2]=0, normal order SA,SB,SC (e.g. RGB) [reset] A[2]=1, reverse order SC,SB,SA (e.g. BGR) A[3]=0, Disable left-right swapping on COM [reset] A[3]=1, Set left-right swapping on COM A[4]=0, Scan from COM0 to COM[N -1] [reset] A[4]=1, Scan from COM[N-1] to COM0. Where N is the multiplex ratio. A[5]=0, Disable COM Split Odd Even [reset] A[5]=1, Enable COM Split Odd Even Refer to Figure 10-5 for details. A[7:6] = 00; 256 color format A[7:6] = 01; 65k color format [RESET] A[7:6] = 10; 256k color format A[7:6] = 11; 256k color 16-bit format 2 If 9-/18-bit mode is selected, color depth will be fixed to 256k regardless of the setting. Refer to Table 8-7 for details.
0 1	A1 A[7:0]	1 A ₇	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Display Start Line	Set display start line register by Row A[7:0]: from 00d to 131d [reset = 0d (00h)] Note ⁽¹⁾ A[7:0] must be set to 0 when using A3h command.
0 1	A2 A[7:0]	1 A ₇	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀	Set Display Offset	Set vertical offset by COM A[7:0]: from 00d to 131d [reset = 0d (00h)]
0 0 0 0	A4 A5 A6 A7	1 1 1 1	0 0 0 0	1 1 1 1	0 0 0 0	0 0 0 0	1 1 1 1	0 0 1 1	0 1 0 1	Set Display Mode	A4h=Normal Display [reset] A5h=Entire Display ON, all pixels turn ON at GS63 A6h=Entire Display OFF, all pixels turn OFF A7h=Inverse Display

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	A8 A[7:0]	1 A ₇	0 A ₆	1 A ₅	0 A ₄	1 A ₃	0 A ₂	0 A ₁	0 A ₀	Set Multiplex Ratio	Set MUX ratio to N+1 Mux N = A[7:0] from 15d to 131d (i.e.16MUX -132 MUX) A[7:0] from 00d to 14d are invalid entry [reset= 131d (83h)]
0 1 1 1 1 1	AB A[7:0] B[7:0] C[7:0] D[7:0] E[4:0]	1 A ₇ B ₇ C ₇ D ₇ *	0 A ₆ B ₆ C ₆ D ₆ *	1 A ₅ B ₅ C ₅ D ₅ *	0 A ₄ B ₄ C ₄ D ₄ E ₄	1 A ₃ B ₃ C ₃ D ₃ E ₃	0 A ₂ B ₂ C ₂ D ₂ E ₂	1 A ₁ B ₁ C ₁ D ₁ E ₁	1 A ₀ B ₀ C ₀ D ₀ E ₀	Dim Mode setting	Configure dim mode setting A[7:0] = Reserved. (Set as 00h) B[7:0] = Contrast setting for Color A, valid range 0 to 255d. C[7:0] = Contrast setting for Color B, valid range 0 to 255d. D[7:0] = Contrast setting for Color C, valid range 0 to 255d. E[4:0] = Pre-charge voltage setting, valid range 0 to 31d.
0 0 0	AC AE AF	1 1 1	0 0 0	1 1 1	0 0 0	1 1 1	1 1 1	0 1 1	0 0 1	Set Display ON/OFF	ACh = Display ON in dim mode AEh = Display OFF (sleep mode) [reset] AFh = Display ON in normal mode Refer to Figure 10-12 for transitions between different modes
0 1	B1 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Phase 1 and 2 period adjustment	A[3:0] : Phase 1 period in N DCLKs. 3~31 DCLKs allowed as follow: A[3:0] Phase 1 period 0000 invalid 0001 3 DCLKs 0010 5 DCLKs 0011 7 DCLKs 0100 9 DCLKs [reset] : : 1111 31 DCLKs A[7:4] : Phase 2 period in N DCLKs. 2~15 DCLKs allowed. A[7:4] Phase 2 period 0000 invalid 0001 invalid 0010 2 DCLKs 0011 3 DCLKs : : 0111 7 DCLKs[reset] : : 1111 15 DCLKs

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	B3 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Display Clock Divider / Oscillator Frequency	A[3:0] Divider DCLK is generated from CLK divided by DIVIDER + 1 (i.e., 1 to 16) [reset=0000b] A[7:4] Fosc frequency Frequency increases as setting value increases [reset=1100b]
0 1	B4 A[3:0]	1 *	0 *	1 *	1 *	0 A ₃	1 A ₂	0 A ₁	0 A ₀	Set Second Pre-charge Period	A[3:0] Set Second Pre-charge Period 0000b 0 DCLKS 0001b 1 DCLKS 0010b 2 DCLKS 0111 7 DCLKS [reset] 1111 15 DCLKS
0 1 1 1 1 1 1 1 1 1 1 1 1 1	B8 A1[3:0] : A7[3:0] A8[4:0] : A15[4:0] A16[5:0] : A31[5:0] A32[6:0] : A63[6:0]	1 * : * * * * * * * * * * * *	0 * : * * * * * * * * * * * *	1 * : * * * * * * * * * * * *	1 * : * * * * * * * * * * * *	1 A13 : A73 A83 : A153 A163 : A313 A323 : A633	0 A12 : A72 A82 : A152 A162 : A312 A322 : A632	0 A11 : A71 A81 : A151 A161 : A311 A321 : A631	0 A10 : A70 A80 : A150 A160 : A310 A320 : A630	Set Gray Scale Table	These 63 parameters define Gray Scale (GS) Table in terms of Gamma Setting A1[3:0]: Gamma Setting for GS1, A2[3:0]: Gamma Setting for GS2, A62[6:0]: Gamma Setting for GS62, A63[6:0]: Gamma Setting for GS63. Note ⁽¹⁾ Input 1d for Gamma Setting 1, 2d for Gamma setting 2, ... ,127d for Gamma Setting 127 ⁽²⁾ 0 < Setting of GS1 < Setting of GS2 < Setting of GS3..... Setting 62 < Setting 63 Refer to Section 8.8 for details.
0	B9	1	0	1	1	1	0	0	1	Enable Linear Gray Scale Table	Reset built in Linear Gray Scale table GS0 = Gamma Setting 0; GS1 = Gamma Setting 2 GS2 = Gamma Setting 4; GS3 = Gamma Setting 6; : GS31 = Gamma Setting 62 GS32 = Gamma Setting 65; GS33 = Gamma Setting 67; : GS62 = Gamma Setting 125; GS63 = Gamma Setting 127; Refer to Section 8.8 for details.

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	BB A[5:1]	1 0	0 0	1 A ₅	1 A ₄	1 A ₃	0 A ₂	1 A ₁	1 0	Set Pre-charge level	Set pre-charge voltage level. All three colors share the same pre-charge voltage. [RESET = 3Eh] A[5:1] Hex code pre-charge voltage 0000 00h 0.10 x V _{CC} : : 1111 3Eh 0.55 x V _{CC}
0 1	BE A[5:2]	1 0	0 0	1 A ₅	1 A ₄	1 A ₃	1 A ₂	1 0	0 0	Set V _{COMH}	Set COM deselect voltage level [reset = 3Ch] A[5:2] = A[5:2] Hex code V_{COMH} 0000 00h 0.51 x V _{CC} 0001 04h 0.53 x V _{CC} 1101 34h 0.79 x V _{CC} 1110 38h 0.81 x V _{CC} 1111 3Ch 0.84 x V _{CC}
0 1 1	C0	1 CBTR3 *	1 CBTR2 *	0 CBTR1 *	0 CBTR0 *	0 CATR3 CCTR3	0 CATR2 CCTR2	0 CATR1 CCTR1	0 CATR0 CCTR0	OTP Write	Program data from MCU to OTP for color coordinate tuning. Details refer to section 10.1.22 "OTP Write (C0h)".
0	E2	1	1	1	0	0	0	1	0	Software Reset	Reset display circuit and stop Graphic Acceleration operations.
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation.
0 1	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A ₂	0 1	1 0	Set Command Lock	A[2]: MCU protection status [RESET = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [RESET] A[2] = 1b, Lock OLED driver IC MCU interface from entering command Note ⁽¹⁾ The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.

Note

⁽¹⁾ "*" stands for "Don't care".

Graphic Acceleration Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	21	0	0	1	0	0 A ₃	0 A ₂	0	1	Draw Line	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[5:0] : Color C of the line F[5:0] : Color B of the line G[5:0] : Color A of the line Note ⁽¹⁾ Please enter all 6 bits for Color setting: E[5:0], F[5:0] and G[5:0] , despite of the color format setting in command A0h
1	A[7:0]	A ₇	A ₆	A ₅	A ₄	B ₃	B ₂	A ₁	A ₀		
1	B[7:0]	B ₇	B ₆	B ₅	B ₄	C ₃	C ₂	B ₁	B ₀		
1	C[7:0]	C ₇	C ₆	C ₅	C ₄	D ₃	D ₂	C ₁	C ₀		
1	D[7:0]	D ₇	D ₆	D ₅	D ₄	E ₃	E ₂	D ₁	D ₀		
1	E[5:0]	*	*	E ₅	E ₄	F ₃	F ₂	E ₁	E ₀		
1	F[5:0]	*	*	F ₅	F ₄	G ₃	G ₂	F ₁	F ₀		
1	G[5:0]	*	*	G ₅	G ₄			G ₁	G ₀		
0	22	0	0	1	0	0 A ₃	0 A ₂	1	0	Drawing Rectangle	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[5:0] : Color C of the line F[5:0] : Color B of the line G[5:0] : Color A of the line H[5:0] : Color C of the fill area I[5:0] : Color B of the fill area J[5:0] : Color A of the fill area Note ⁽¹⁾ Please enter all 6 bits for Color setting: E[5:0], F[5:0] , G[5:0], H[5:0]. I[5:0] and J[5:0] , despite of the color format setting in command A0h ⁽²⁾ 0<A[7:0] < C[7:0] <159 ⁽³⁾ 0<B[7:0] < D[7:0]<131
1	A[7:0]	A ₇	A ₆	A ₅	A ₄	B ₃	B ₂	A ₁	A ₀		
1	B[7:0]	B ₇	B ₆	B ₅	B ₄	C ₃	C ₂	B ₁	B ₀		
1	C[7:0]	C ₇	C ₆	C ₅	C ₄	D ₃	D ₂	C ₁	C ₀		
1	D[7:0]	D ₇	D ₆	D ₅	D ₄	E ₃	E ₂	D ₁	D ₀		
1	E[5:0]	*	*	E ₅	E ₄	F ₃	F ₂	E ₁	E ₀		
1	F[5:0]	*	*	F ₅	F ₄	G ₃	G ₂	F ₁	F ₀		
1	G[5:0]	*	*	G ₅	G ₄	H ₃	H ₂	G ₁	G ₀		
1	H[5:0]	*	*	H ₅	H ₄	I ₃ J ₃	I ₂ J ₂	H ₁	H ₀		
1	I[5:0]	*	*	I ₅	I ₄			I ₁	I ₀		
1	J[5:0]	*	*	J ₅	J ₄			J ₁	J ₀		
0	23	0	0	1	0	0 A ₃	0 A ₂	1	1	Copy	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End E[7:0] : Column Address of New Start F[7:0] : Row Address of New Start
1	A[7:0]	A ₇	A ₆	A ₅	A ₄	B ₃	B ₂	A ₁	A ₀		
1	B[7:0]	B ₇	B ₆	B ₅	B ₄	C ₃	C ₂	B ₁	B ₀		
1	C[7:0]	C ₇	C ₆	C ₅	C ₄	D ₃	D ₂	C ₁	C ₀		
1	D[7:0]	D ₇	D ₆	D ₅	D ₄	E ₃	E ₂	D ₁	D ₀		
1	E[7:0]	E ₇	E ₆	E ₅	E ₄	F ₃	F ₂	E ₁	E ₀		
1	F[7:0]	F ₇	F ₆	F ₅	F ₄			F ₁	F ₀		
0	24	0	0	1	0	0 A ₃	1 A ₂	0	0	Dim Window	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End The effect of dim window: GS15~GS0 no change GS19~GS16 become GS4 GS23~GS20 become GS5 ... GS63~GS60 become GS15
1	A[7:0]	A ₇	A ₆	A ₅	A ₄	B ₃	B ₂	A ₁	A ₀		
1	B[7:0]	B ₇	B ₆	B ₅	B ₄	C ₃	C ₂	B ₁	B ₀		
1	C[7:0]	C ₇	C ₆	C ₅	C ₄	D ₃	D ₂	C ₁	C ₀		
1	D[7:0]	D ₇	D ₆	D ₅	D ₄			D ₁	D ₀		

Graphic Acceleration Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1 1 1	25 A[7:0] B[7:0] C[7:0] D[7:0]	0 A ₇ B ₇ C ₇ D ₇	0 A ₆ B ₆ C ₆ D ₆	1 A ₅ B ₅ C ₅ D ₅	0 A ₄ B ₄ C ₄ D ₄	0 A ₃ B ₃ C ₃ D ₃	1 A ₂ B ₂ C ₂ D ₂	0 A ₁ B ₁ C ₁ D ₁	1 A ₀ B ₀ C ₀ D ₀	Clear Window	A[7:0] : Column Address of Start B[7:0] : Row Address of Start C[7:0] : Column Address of End D[7:0] : Row Address of End
0 1	26 A[4:0]	0 *	0 *	1 *	0 A ₄	0 0	1 0	1 0	0 A ₀	Fill Enable / Disable	A[0] : 0b = Disable Fill for Draw Rectangle Command [reset] 1b = Enable Fill for Draw Rectangle Command A[3:1] : 000 (Reserved values) A[4] : 0b = Disable reverse copy (reset) 1b = Enable reverse during copy command.
0 1 1 1 1 1	27 A[7:0] B[7:0] C[7:0] D[7:0] E[1:0]	0 A ₇ B ₇ C ₇ D ₇ *	0 A ₆ B ₆ C ₆ D ₆ *	1 A ₅ B ₅ C ₅ D ₅ *	0 A ₄ B ₄ C ₄ D ₄ *	0 A ₃ B ₃ C ₃ D ₃ *	1 A ₂ B ₂ C ₂ D ₂ *	1 A ₁ B ₁ C ₁ D ₁ E ₁	1 A ₀ B ₀ C ₀ D ₀ E ₀	Continuous Horizontal & Vertical Scrolling Setup	A[7:0]: Set number of column as horizontal scroll offset Range: 0d-131d (no horizontal scroll if equals to 0 B[7:0]: Define start row address C[7:0]: Set number of rows to be horizontal scrolled B[7:0]+C[7:0] <=132 D[7:0]: Set number of row as vertical scroll offset Range: 0d-131d (no vertical scroll if equals to 0) E[1:0]: Set time interval between each scroll step 00b 3 frames 01b 5 frames 10b 50 frames 11b 100 frames Note: ⁽¹⁾ Vertical scroll run with command A3h Set Vertical Scroll Area ⁽²⁾ The parameters should not be changed after scrolling is activated
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Deactivate horizontal scrolling. Note ⁽¹⁾ After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

Graphic Acceleration Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Activate horizontal scrolling. This command activates the scrolling function according to the setting done by command 27h Continuous Horizontal & Vertical Scrolling Setup
0 1 1	A3 A[7:0] B[7:0]	1 A7 B7	0 A6 B6	1 A5 B5	0 A4 B4	0 A3 B3	0 A2 B2	1 A1 B1	1 A0 B0	Set Vertical Scroll Area	A[7:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[7:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 132] Note ⁽¹⁾ A[7:0]+B[7:0] <= MUX ratio ⁽²⁾ B[7:0] <= MUX ratio ⁽³⁾ Set Display Start Line (A1h) must be set to 0 when using A3h command. ⁽⁴⁾ The last row of the scroll area shifts to the first row of the scroll area. ⁽⁵⁾ For 132d MUX display A[7:0] = 0, B[7:0]=132 : whole area scrolls A[7:0]= 0, B[7:0] < 132 : top area scrolls A[7:0] + B[7:0] < 132 : central area scrolls A[7:0] + B[7:0] = 132 : bottom area scrolls Refer to Figure 10-20 for details.

12. Reliability

Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	—
2	High temp. (Operation)	70°C, 120hrs	—
3	Low temp. (Operation)	-40°C, 120hrs	—
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 120hrs	—
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles.	—
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	—
7	Drop	Height: 120cm Sequence : 1 angle、 3 edges and faces Cycles: 1	—
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	—

13. Appendix (Drawing)

