

(NPN) MJ11028, MJ11030, MJ11032 (PNP) MJ11029, MJ11033

High-Current Complementary Silicon Power Transistors

... for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain –
 $h_{FE} = 1000$ (Min) @ $I_C = 25$ Adc
 $h_{FE} = 400$ (Min) @ $I_C = 50$ Adc
- Curves to 100 A (Pulsed)
- Diode Protection to Rated I_C
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor
- Junction Temperature to +200°C

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|----------------|-----------------|---------------|
| Collector-Emitter Voltage MJ11028/29 MJ11030 MJ11032/33 | V_{CEO} | 60 90 120 | Vdc |
| Collector-Base Voltage MJ11028/29 MJ11030 MJ11032/33 | V_{CBO} | 60 90 120 | Vdc |
| Emitter-Base Voltage | V_{EBO} | 5.0 | Vdc |
| Collector Current – Continuous – Peak (Note 1) | I_C | 50 100 | Adc |
| Base Current – Continuous | I_B | 2.0 | Adc |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above 25°C @ $T_C = 100^\circ\text{C}$ | P_D | 300 1.71 | Watts W/°C |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | -5 5 to +200 | °C |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|--|-----------------|------|------|
| Maximum Lead Temperature for Soldering Purposes for ≤ 10 seconds | T_L | 275 | °C |
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 0.58 | °C/W |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

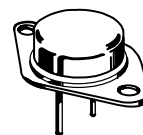
1. Pulse Test: Pulse Width = 5 μs , Duty Cycle $\leq 10\%$.



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**50 AMPERE
COMPLEMENTARY
DARLINGTON POWER
TRANSISTORS
60 – 120 VOLTS
300 WATTS**



TO-204 (TO-3)
CASE 197A
STYLE 1

MARKING DIAGRAM



xx = 28, 29, 30, 32, 33
A = Location Code
YY = Year
WW = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
|---------|---------|----------------|
| MJ110xx | TO-204 | 100 Units/Tray |

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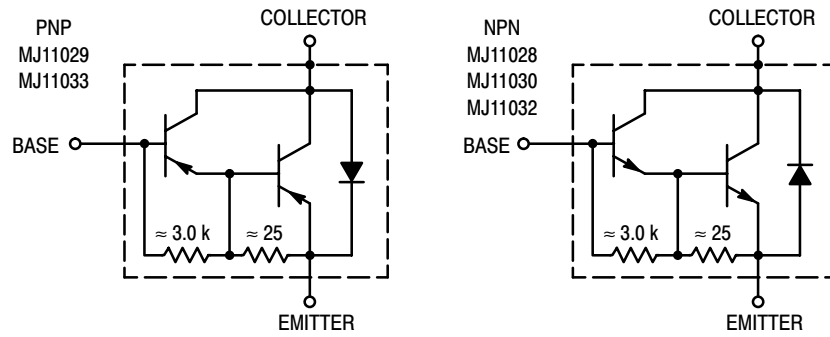


Figure 1. Darlington Circuit Schematic

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---------------|-----------------------|-------------------------|------|
| OFF CHARACTERISTICS | | | | |
| Collector–Emitter Breakdown Voltage (Note 1) ($I_C = 1.00\text{ mA}$, $I_B = 0$) | $V_{(BR)CEO}$ | 60 90 120 | — | Vdc |
| Collector–Emitter Leakage Current ($V_{CE} = 60\text{ Vdc}$, $R_{BE} = 1\text{ k}\Omega$) ($V_{CE} = 90\text{ Vdc}$, $R_{BE} = 1\text{ k}\Omega$) ($V_{CE} = 120\text{ Vdc}$, $R_{BE} = 1\text{ k}\Omega$) ($V_{CE} = 60\text{ Vdc}$, $R_{BE} = 1\text{ k}\Omega$, $T_C = 150^\circ\text{C}$) ($V_{CE} = 120\text{ Vdc}$, $R_{BE} = 1\text{ k}\Omega$, $T_C = 150^\circ\text{C}$) | I_{CER} | — — — — — | 2 2 2 10 10 | mAdc |
| Emitter Cutoff Current ($V_{BE} = 5\text{ Vdc}$, $I_C = 0$) | I_{EBO} | — | 5 | mAdc |
| Collector–Emitter Leakage Current ($V_{CE} = 50\text{ Vdc}$, $I_B = 0$) | I_{CEO} | — | 2 | mAdc |
| ON CHARACTERISTICS (Note 1) | | | | |
| DC Current Gain ($I_C = 25\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 50\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) | h_{FE} | 1 k 400 | 18 k — | — |
| Collector–Emitter Saturation Voltage ($I_C = 25\text{ Adc}$, $I_B = 250\text{ mA}$) ($I_C = 50\text{ Adc}$, $I_B = 500\text{ mA}$) | $V_{CE(sat)}$ | — — | 2.5 3.5 | Vdc |
| Base–Emitter Saturation Voltage ($I_C = 25\text{ Adc}$, $I_B = 200\text{ mA}$) ($I_C = 50\text{ Adc}$, $I_B = 300\text{ mA}$) | $V_{BE(sat)}$ | — — | 3.0 4.5 | Vdc |

1. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

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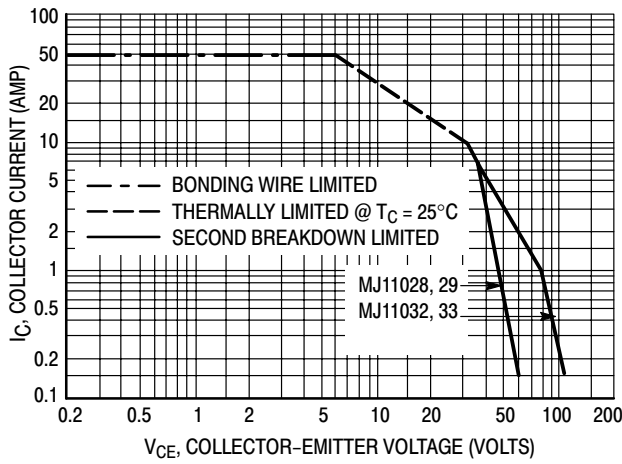


Figure 2. DC Safe Operating Area

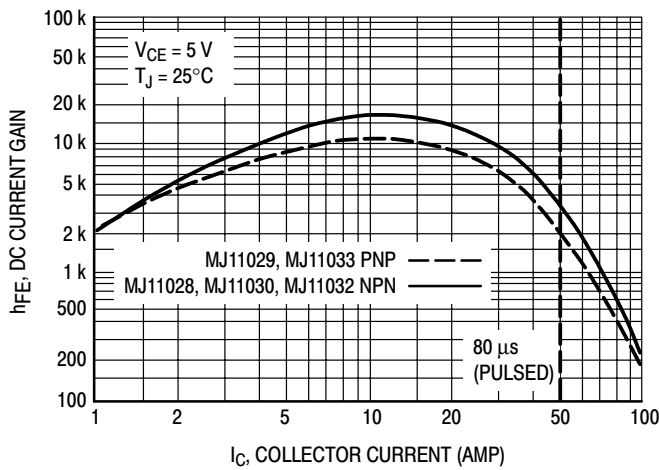


Figure 3. DC Current Gain

There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

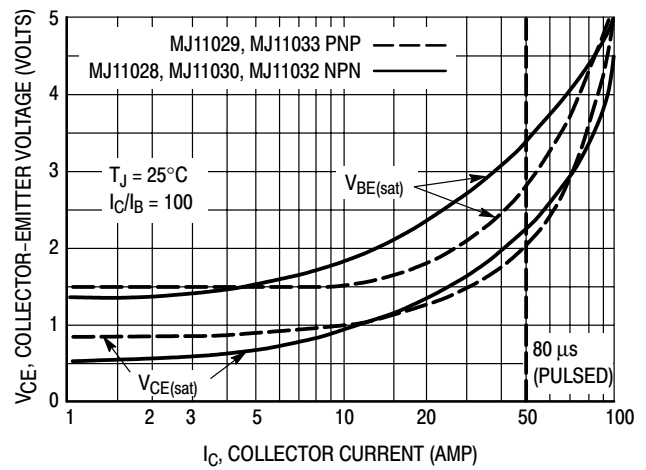
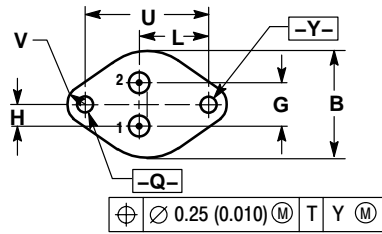
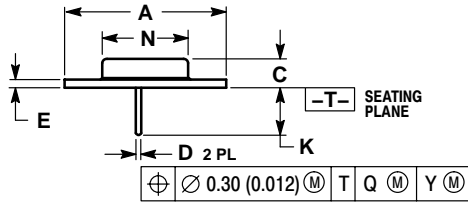


Figure 4. "On" Voltage

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PACKAGE DIMENSIONS

TO-204 (TO-3)
CASE 197A-05
ISSUE K



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.530 REF | | 38.86 REF | |
| B | 0.990 | 1.050 | 25.15 | 26.67 |
| C | 0.250 | 0.335 | 6.35 | 8.51 |
| D | 0.057 | 0.063 | 1.45 | 1.60 |
| E | 0.060 | 0.070 | 1.53 | 1.77 |
| G | 0.430 BSC | | 10.92 BSC | |
| H | 0.215 BSC | | 5.46 BSC | |
| K | 0.440 | 0.480 | 11.18 | 12.19 |
| L | 0.665 BSC | | 16.89 BSC | |
| N | 0.760 | 0.830 | 19.31 | 21.08 |
| Q | 0.151 | 0.165 | 3.84 | 4.19 |
| U | 1.187 BSC | | 30.15 BSC | |
| V | 0.131 | 0.188 | 3.33 | 4.77 |

STYLE 1:

- PIN 1: BASE
2: EMITTER
CASE: COLLECTOR

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